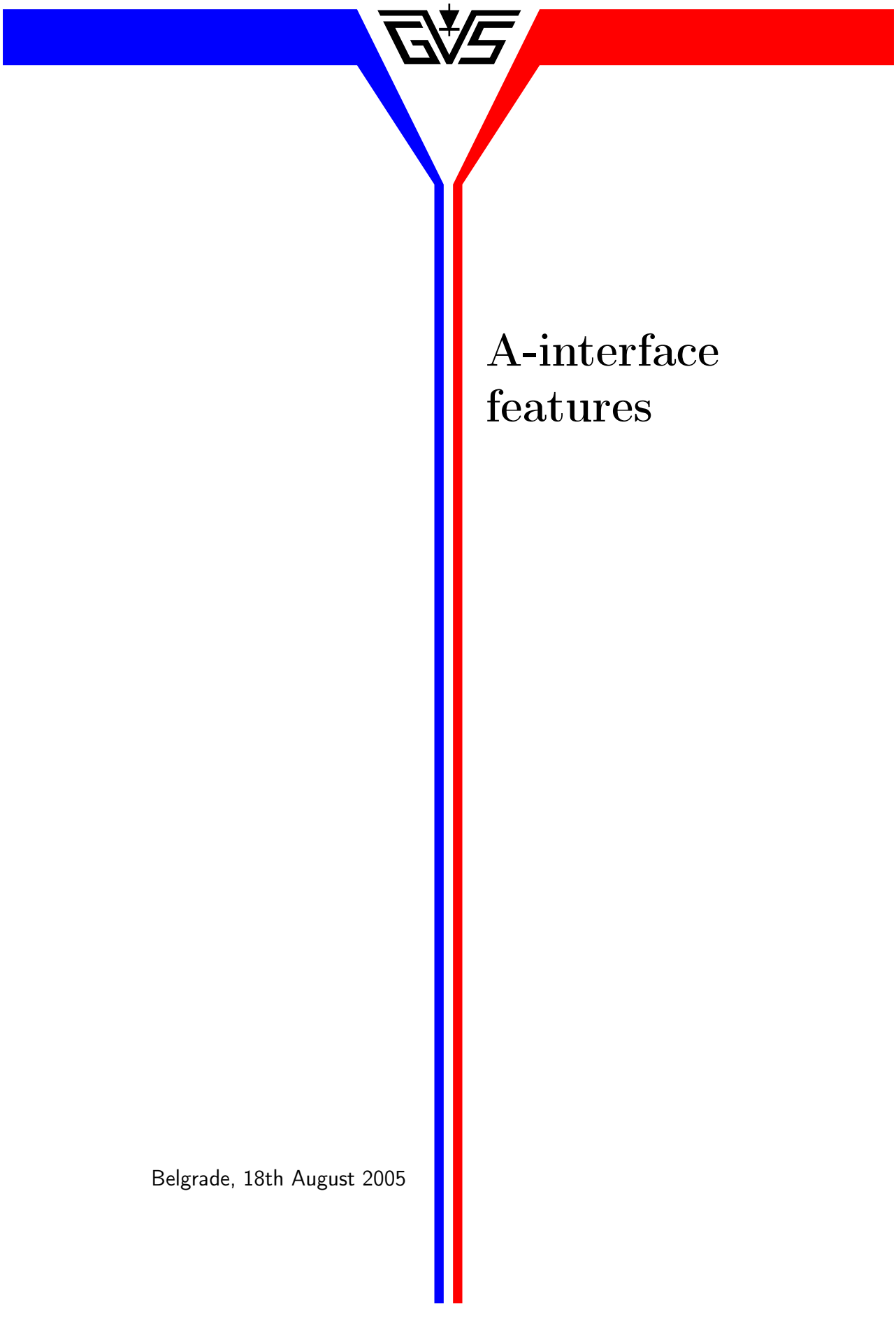

A-interface features

Belgrade, 18th August 2005

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1 Basic characteristics

Bit rate: 2048 kbit/s ± 50 ppm (in accordance with ITU-T G.703, §6.1) Code: High density bipolar of order 3 (HDB3) (in accordance with ITU-T G.703, §6.1)

1.1 Overvoltage protection:

In accordance with Recommendation K20.

2 Output port characteristics

Output port signal characteristics are demonstrated in the following table (in accordance with ITU-T G.703,§6.2, table 6.):

Pulse form (nominally rectangular)	Valid pulse geometry is specified in figure 1, regardless of signal polarity	
Connecting cable type	Coaxial cable	Symmetrical pair
Impedance	75Ω resistive	120Ω resistive
Nominal voltage (pulse)	2.37 V	3 V
Nominal voltage (pause)	0±0.237V	0±0.3V
Nominal pulse width	244ns	
Ratio of the amplitudes of positive and negative pulses at the center of pulse interval	0.95 to 1.05	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	
Maximum peak-to-peak jitter at the output port	1.5UI from 20Hz to 18kHz 0.2UI from 18Hz to 100kHz in accordance with Recommendation ITU-T G.823,§2	

Table 1: *Output port characteristics*

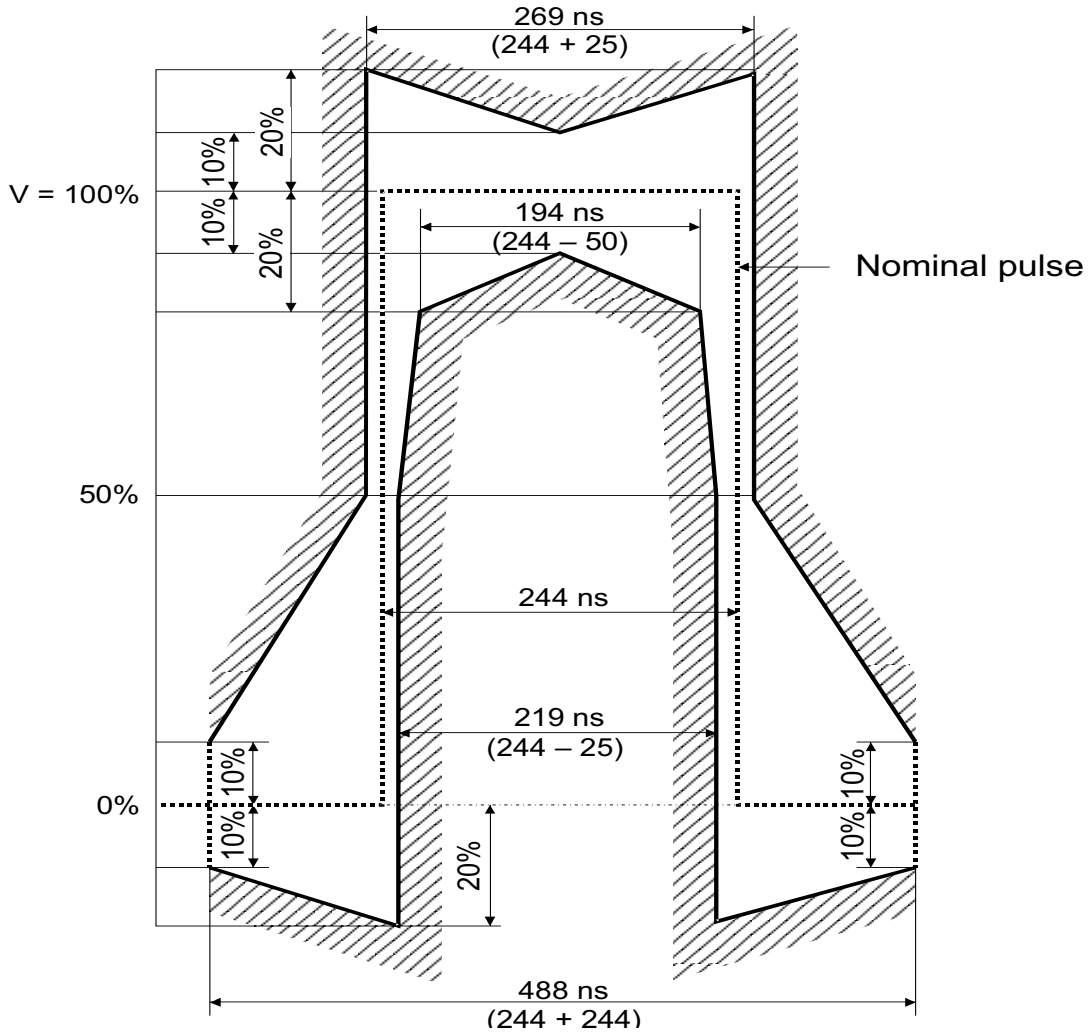

Figure 1: *A-interface pulse form*

3 Input port characteristics

Input signal is modified in accordance with connecting cable characteristics. It may be assumed that cable loss conforms with $f^{1/2}$ law, remaining in 0 - 6 dB range at 1024KHz frequency (in accordance with Recommendation ITU-T G.703,§6.3.1).

3.1 Maximum input jitter

Maximum tolerated input jitter is presented on the graphic below (in accordance with ITU-T G.823,§3):

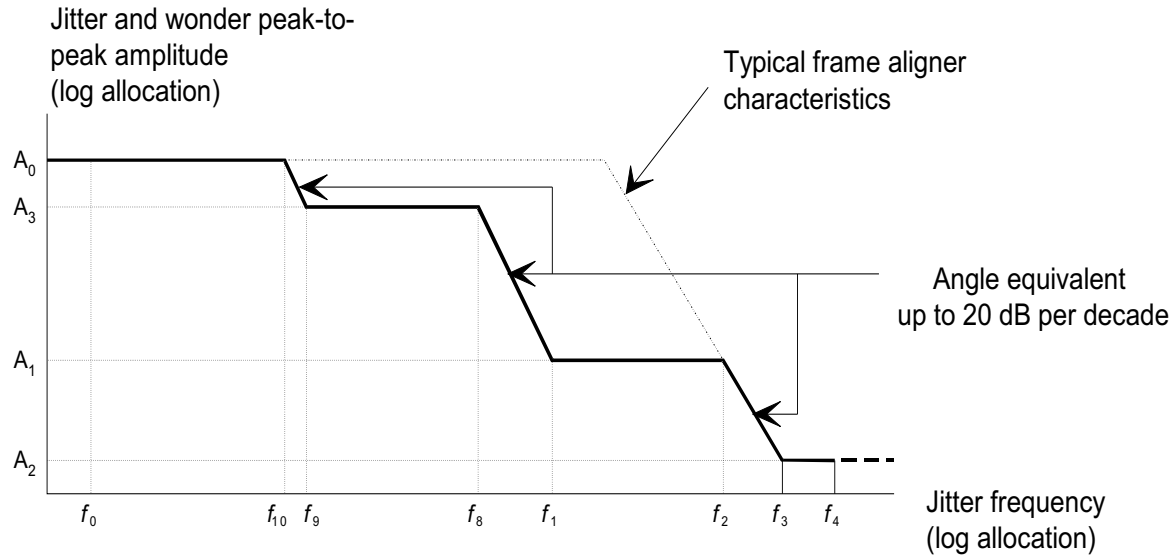

Figure 2: *Maximum jitter and wander lower bound at the input port*

Specific graphic values are presented in the table:

Peak-to-peak amplitude unit interval				Frequency								PSR test signal
A_0	A_1	A_2	A_3	f_0	f_{10}	f_9	f_8	f_1	f_2	f_3	f_4	
36.9	18	1.5	0.2	1.2x10^{-5}	4.88x10^{-3}	0.01	1.667	20	2400	18000	100000	2^{15}-1

Table 2: *Parameters of the maximum jitter lower bound at the input port*

3.2 Input port return loss

The following presented are minimum values of input port return loss (in accordance with ITU-T G.703, §6.3.3.):

Frequency range [kHz]	Return loss [dB]
51-102	12
102-2048	18
2048-3072	14

Table 3: *Input port return loss*

3.3 Shield (external conductor) grounding

The external conductor of coaxial cable or symmetrical pair (shield) is grounded at the output port. The option of reception port grounding, when needed, is also provided (in accordance with ITU-T G.703, §6.4.)

4 Multiplex organization

4.1 Frame length

Frame length is 256 bits. The frame repetition rate is 8000Hz. (in accordance with Recommendation ITU-T G.704, §2.3.1)

4.2 Allocation of bits number 1 to 8 of the frame

Bit allocation is presented in the following table (in accordance with Recommendation ITU-T G.704, §2.3.2):

Alternate frames	1	2	3	4	5	6	7	8
Frame containing	S_i	0	0	1	1	0	1	1
FAS signal	Frame Alignment Signal							
Frame not containing	S_i	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
FAS signal								

Table 4: *Allocation of bits 1 to 8 of PCM frame*

S_i bits are reserved for the international use. These bits may be used for CRC-4 procedure. When not used, bits should be fixed to binary 1, provided that the link is crossing the interna-

tional border. When not crossing the international borders, bits are left free for national use, as regulated.

A bit is Remote Alarm Indication (RAI) bit. It is set to 1 in alarm conditions (frame alignment signal loss); in undisturbed operation, set to 0.

Bits S_{a4}... S_{a8} may be used for any of following purposes:

- in specific point-to-point applications conforming to CCITT recommendations and related to transcoder equipment (G.761) for alarm state indication
- S_{a4} bit may be used as a message-based data link for maintenance and monitoring. With post-set S_{a4} bits, this operation is performed with CRC-4 procedure retained.
- S_{a5}...S_{a7} bits are for national usage when there is no demand for specific point-to-point applications
- S_{a4},..., S_{a8} bits are set to 1 (when not used) on links crossing an international border

4.3 Description of CRC-4 procedure in bit 1 position of PCM frame (in accordance with Recommendation ITU-T G.704, §2.3.3)

Where there is a need to provide additional protection against simulation of the frame alignment signal, and/or where there is a need for an enhanced error monitoring capability, then bit 1 of each frame should be used for a cyclic redundancy check-4 (CRC-4) procedure.

Equipment incorporating the CRC-4 procedure should be designed to be capable to provide service (traffic) between equipments with and without a CRC-4 capability. This can be achieved either manually or automatically:

- For the manual case, the equipment incorporating the CRC-4 procedure should be capable of fixing CRC-4 bits to the binary "1" state

- For the automatic case, this function implies the possibility to request the equipment operation without CRC-4 procedure from a higher layer or to obtain equipment operation with no CRC-4 procedure operation ability using modified CRC-4 algorithm.

4.3.1 CRC-4 multiframe description

The table below presents CRC-4 multiframe.

	Sub-	Frame	Bits 1 to 8 of the frame							
	-multiframe	number	1	2	3	4	5	6	7	8
Multiframe	1	0	C_1	0	0	1	1	0	1	1
		1	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		2	C_2	0	0	1	1	0	1	1
		3	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		4	C_3	0	0	1	1	0	1	1
		5	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		6	C_4	0	0	1	1	0	1	1
		7	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	2	8	C_1	0	0	1	1	0	1	1
		9	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		10	C_2	0	0	1	1	0	1	1
		11	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		12	C_3	0	0	1	1	0	1	1
		13	E	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		14	C_4	0	0	1	1	0	1	1
		15	E	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}

Table 5: *CRC-4 multiframe*

C_1,..., C_4 bits represent CRC-4 bits. E bits are CRC-4 error indications bits.

Each CRC-4 multiframe is divided in 16 frames marked with numbers 0 to 15. These 16 frames are divided into two 8-frame sub-multiframes. Each sub-multiframe has a CRC-4 block size (2048 bits).

4.3.2 Use of bit 1 in the frame

In those frames containing the frame alignment signal, bits marked with number 1 are used to transmit the CRC-4 bits (C_1,..., C_4). There are 4 CRC-4 bits in each sub-multiframe.

In those frames not containing the frame alignment signal, bit 1 is used to transmit the 6-bit CRC-4 multiframe alignment signal with form 001011 as well as two CRC-4 error indication bits (E).

The E-bits should be set to "0" until both basic frame and CRC-4 multiframe alignment are established.Thereafter, the E-bits should be used to indicate received errored sub-multiframes by setting the binary state of one E-bit from 1 to 0 for each errored sub-multiframe.

Any delay between the detection of an errored sub-multiframe and the setting of the E-bit that indicates the error state must be less than 1 second.

The E-bits will always be taken into account even if the received SMF is found to be errored, since there is little likelihood that the E-bits themselves will be errored.

When the remote equipment is found not using E bits, there should be provided an option for setting the E bits to binary 1.

4.3.3 CRC

CRC bits are generated as shown in the following figure (in accordance with ITU-T G.704, §2.3.3.5.):

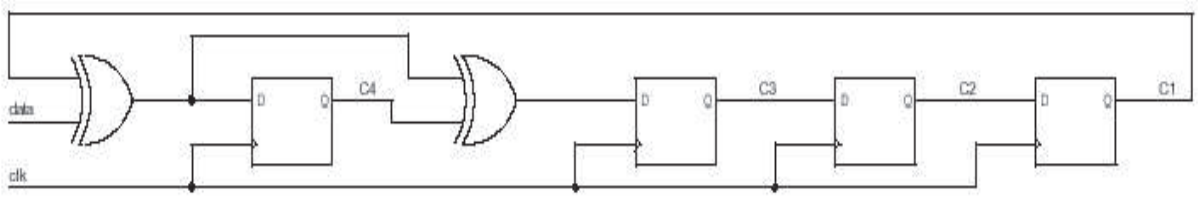

Figure 3: *CRC-4 bit generating*

4.3.3.1. Encoding process

Encoding process is conveyed as presented below (in accordance with ITU-T G.704, §2.3.3.5.2.):

- bits C_1,..., C_4 in sub-multiframe are set to binary 0
- all sub-multiframes are acted upon as shown in the previous figure
- after having the last sub-multiframe bit stored in the first FF from the previous figure, C_1,..., C_4 bits are obtained and allocated to appropriate position within following CRC-4 sub-multiframe.

4.3.3.2. Decoding process

Decoding process is conveyed as presented below (in accordance with ITU-T G.704, §2.3.3.5.3.):

- A received CRC-4 sub-multiframe is acted upon as demonstrated in the previous figure, extracting CRC-4 bits and replacing them by 0s.

- After having the last CRC-4 sub-multiframe bit stored in the first FF from the previous figure, C_1,..., C_4 bits are obtained and compared with the CRC-4 bits extracted from the subsequent CRC-4 sub-multiframe.

- If the CRC-4 bits are identical, it is assumed that the received CRC-4 sub-multiframe is error free.

5 Frame alignment and CRC-4 procedure

5.1 Loss and recovery of frame alignment signal

5.1.1 Frame alignment signal loss (in accordance with ITU-T G.706, §4.1.1.)

Frame alignment will be assumed to have been lost after having received three consecutive incorrect frame alignment signals. In addition, frame alignment will be assumed to have been lost when bit 2 in frames not containing the frame alignment signal has been received with an error on three consecutive occasions.

When CRC-4 multiframe alignment procedure fails to complete within time specified, frame alignment will be assumed lost.

5.1.2 Strategy for frame alignment recovery (conforming with ITU-T G.706, §4.1.2.)

Frame alignment will be assumed to have been recovered when the following procedure is completed:

- for the first time, the presence of the correct frame alignment signal is detected in frame n
- the absence of FAS signal is detected in frame (n+1) verifying that bit 2 is a 1
- the presence of the correct frame alignment signal in (n+2) frame is detected.

To avoid the possibility of a state in which no frame alignment can be achieved due to the presence of a spurious frame alignment signal, it is necessary to start the new search for valid FAS signal in frame n+2.

5.2 CRC-4 multiframe alignment using bit 1 (conforming with ITU-T G.706, §4.2.)

CRC-4 Frame alignment will be assumed to have been achieved if at least two valid CRC multiframe alignment signals can be located within 8 ms, the time separating two CRC multiframe alignment signals being 2 ms or a multiple of 2 ms.

The search for the CRC-4 MFAS should be made in the frame not containing the frame alignment signal.

If CRC-4 multiframe alignment cannot be achieved within 8 ms, it should be assumed that the cause was a spurious frame alignment signal and another search should be initiated.

If CRC-4 multiframe alignment cannot be achieved within time interval of 100-500ms consequent actions should be taken equivalent to those specified for loss of frame alignment.

5.2.1 Operation with equipment not supporting CRC-4 procedure (conforming to ITU-T G.706, Annex B)

Modified CRC-4 alignment algorithm shown in figure 4 is applied.

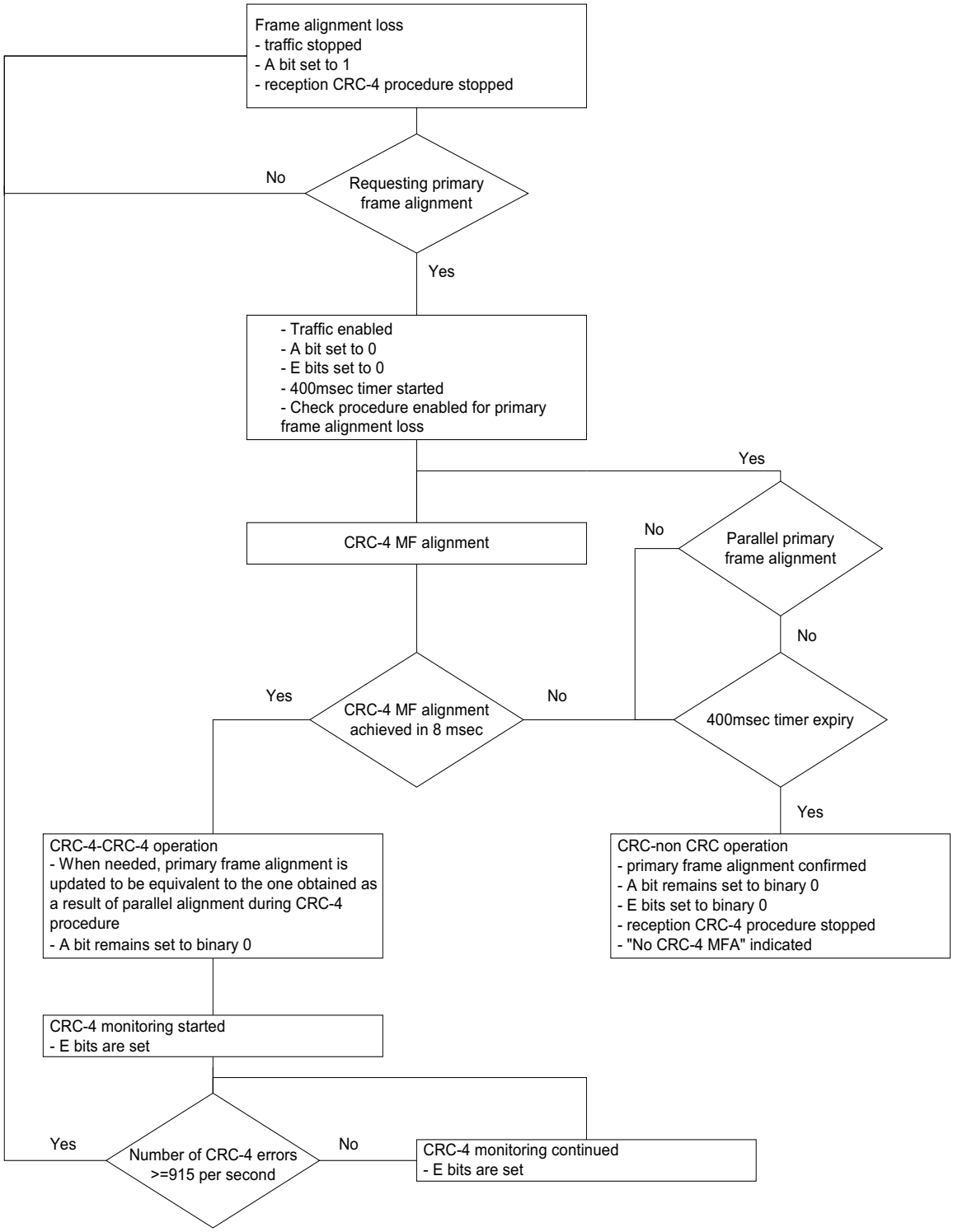

Figure 4: *Modified CRC-4 alignment algorithm*

6 Frame structures carrying channels at various bit rates in 2048 kbit/s interfaces

6.1 Interface carrying 64Kbit/s channels

6.1.1 Frame structure (conforming with ITU-T G.704, §5.1.)

Number of bits per each 64Kbit/s channel time slot is 8, numbered 1 to 8.

Each frame contains 32 64Kbit/s channel time slots, 256 bits total.

0 channel is used as described in section 4.

Each of channel time slots 1 to 15 and 17 to 31 can accommodate PCM-encoded voiceband signal samples.

Channel 16 may be used for signalling. If not needed for signalling, channel 16 may be used the same way as channels slots 1,..., 15 and 17,..., 31.

6.1.2 Signalling

The use of 64 kbit/s channel time slot 16 is recommended for either CCS or CAS signalling as required.

6.1.3 Common channel signalling

Channel time slot 16 may be used for communication up to a rate of 64 kbit/s.

6.1.4 Channel associated signalling

In this case, frames are arranged into multiframes the way described in section 4. Bits 1 to 4 of the channel time slot in 0 multiframe are set to 0 and are used for multiframe alignment.

Following table presents bit allocation of 16 channel time slot for CAS purposes.

Channel 16 of frame 0	Channel 16 of frame 1		Channel 16 of frame 2		Channel 16 of frame 3		... ...	Channel 16 of frame 15	
0000xyxx	abcd ch. 1	abcd ch. 17	abcd ch. 2	abcd ch. 18	abcd ch. 3	abcd ch. 19	... ...	abcd ch. 15	abcd ch. 31

Table 6: *Channel 16 bit allocation*

6.2 Interface carrying n x 64 kbit/s channels (conforming with ITU-T G.704, §5.2.)

6.2.1 Channel 0

Channel 0 is filled the same as mentioned in 4.2.

6.2.2 Channel 16

Channel 16 is reserved for signalling purposes, if needed.

6.2.3 Remaining channels

If 2<=n<=15, TS_1 to TS_n are filled with n x 64Kbit/s data.
If 15<n<=30 , TS_1 to TS_{15} and TS_{17} to $TS_{(n=1)}$ are filled with n x 64Kbit/s data.
Remaining channels are filled with binary 1s.

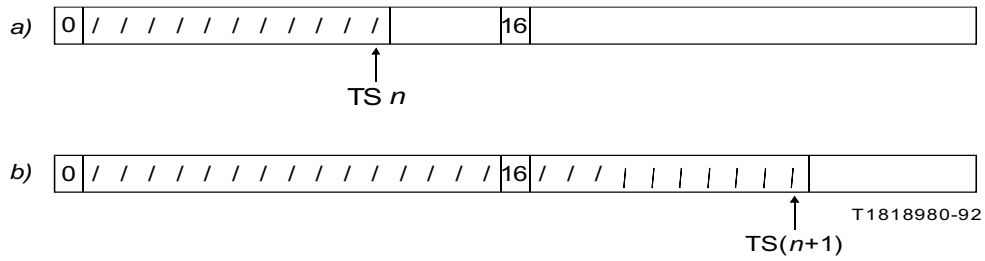

Figure 5: *Filling of frame with one n x 64Kbit/s signal*

6.3 Interface with one or more n x 64Kbit/s signals on the multiplexed signal side

For any one n x 64 kbit/s signal, time slots of the 2048 kbit/s frame are filled as follows:

6.3.1 Channel 0

Channel 0 is filled the same as mentioned in 4.2.

6.3.2 Channel 16

Channel 16 is reserved for signalling purposes, if needed.

6.3.3 Remaining channels

TS(x) is designated as the time slot into which the first time slot of the n x 64 kbit/s is accommodated.

If x<=15 and x+n-1<=15, or of x>=17 and x+n-1<=31 then the filling of frame is shown in figures 6 a and 6 б.

If x+n-1>=16 then the filling of time slots from TS(x) to TS(15) and TS(17) to TS(x+n) is shown in figure 6 c.

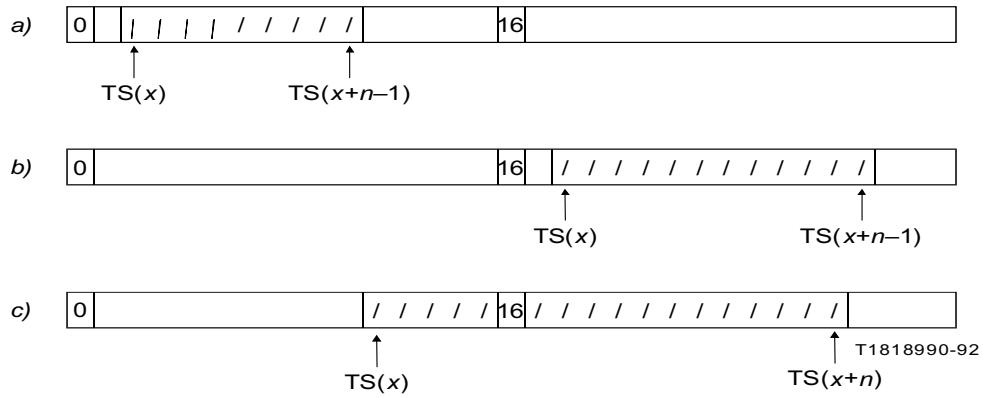

Figure 6: *Filling of frame with one or more n x 64Kbit/s signals*

7 Loss and recovery of frame alignment signal in CAS signalling

Frame alignment is assumed to have been lost if there were two consecutive frame alignment signals received errored.

Frame alignment is assumed to have been achieved on receiving the first correct multiframe alignment signal.

To avoid incorrect multiframe alignment, following procedures should be conveyed:

- frame alignment is assumed to have been lost if all 16 channels with all 0 bits are received in one or two multiframes.

- frame alignment is assumed to have been achieved if there is at least one bit 0 of the channel 16 in the frame preceding to the one with first correct multiframe alignment signal detected.