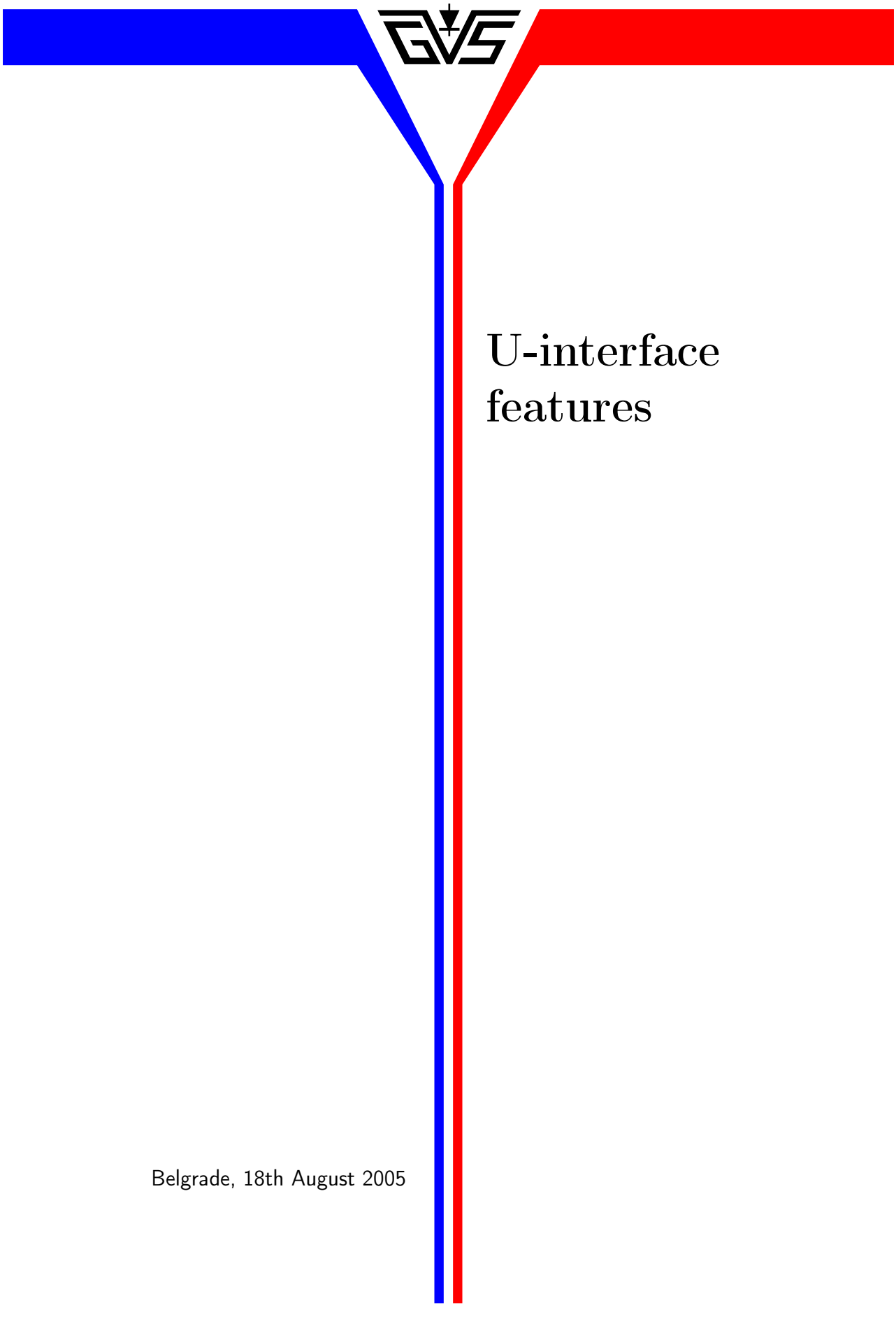

U-interface features

Belgrade, 18th August 2005

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1 Basic characteristics

1.1 Bit rate

80 kbauds ± 5 ppm (in accordance with ITU-T G.961, Appendix II §II.2)

1.2 Line code

2B1Q (in accordance with ITU-T G.961, Appendix II §II.1)
This is a 4-level code without redundancy. The B- and D-channels are scrambled before coding. M_1 to M_6 C_L channel bits are coded and scrambled just the same. Bits are grouped into pairs of bits for conversion to quaternary symbols that are called quats. The following table presents B- and D-channel bit conversion to quats.

First bit (sign)	Second bit (magnitude)	Quaternary symbol (quat)
1	0	+3
1	1	+1
0	1	-1
0	0	-3

Table 1: *Conversion of pairs of bits to quaternary symbols*

At the receiver, quaternary symbols are converted to pairs of bits and descrambled.

1.3 Impedance

135Ω symmetrically (in accordance with ITU-T G.961, Appendix II §II.13.1.)

2 Interface output characteristics

Nominal maximum signal value at the line terminal is 2.5V (in accordance with ITU-T G.961, Appendix II §II.12.1.).

2.1 Pulse shape

Pulse shape is specified in the figure below (in accordance with ITU-T G.961, Appendix II §II.12.2.).

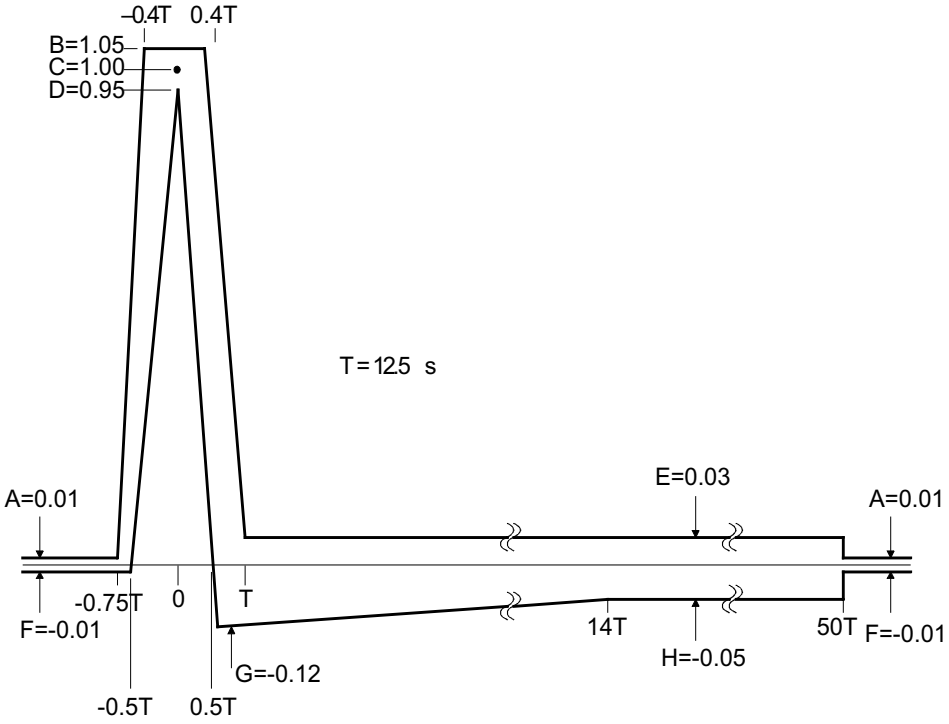

Figure 1: *Transmitter pulse shape*

Normalized level		Quaternary symbols			
		+3	+1	-1	-3
A	0.01	0.025V	0.008330V	-0.008330V	-0.025V
B	1.05	2.625V	0.875000V	-0.875000V	-0.025V
C	1.00	2.500V	5/6V	-5/6V	-2.500V
D	0.95	2.375V	0.791670V	-0.791670V	-2.375V
E	0.03	0.075V	0.025000V	-0.025000V	-0.075V
F	-0.01	-0.025V	-0.008330V	0.008330V	0.025V
G	-0.12	-0.300V	-0.100000V	0.100000V	0.300V
H	-0.05	-0.125V	-0.041670V	0.041670V	0.125V

Table 2: *Transmitter pulse shape*

2.2 Signal power

For a signal consisting of a framed sequence of symbols with a frame word and equiprobable symbols at all other positions, the average symbol power should be between 13.0 dBm and 14.0 dBm over the frequency band from 0 Hz to 80 kHz (in accordance with ITU-T G.961, Appendix II §II.12.3.).

2.3 Power spectral density

The upper bound of the power spectral density is shown in the following figure (in accordance with ITU-T G.961, Appendix II §II.12.4.).

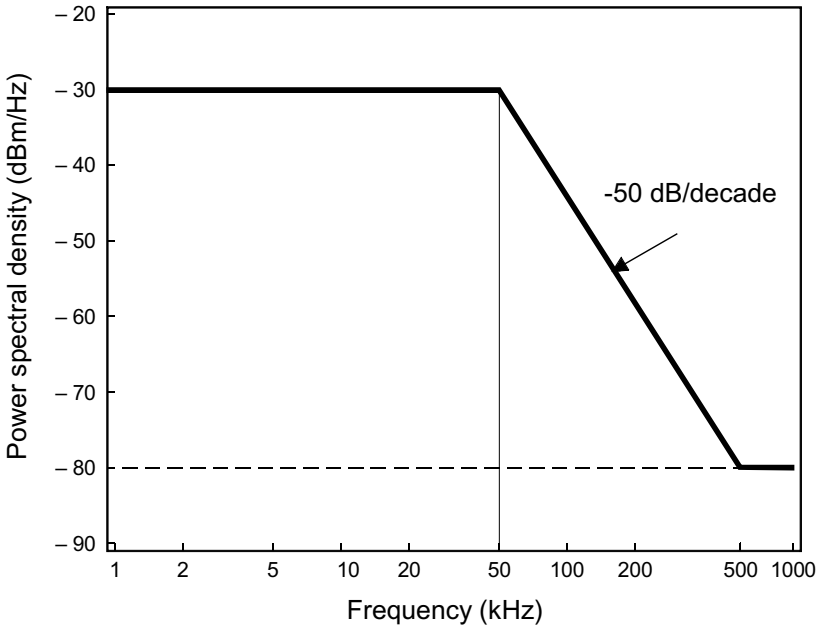

Figure 2: *Line terminal power spectral density*

3 Transmitter/receiver termination

3.1 Impedance

The nominal impedance shall be 135Ω (in accordance with ITU-T G.961, Appendix II §II.13.1.).

3.2 Return loss

Minimum return loss with respect to 135Ω impedance over a frequency band from 1kHz to 200kHz are shown in the following figure (in accordance with ITU-T G.961, Appendix II §II.13.2.).

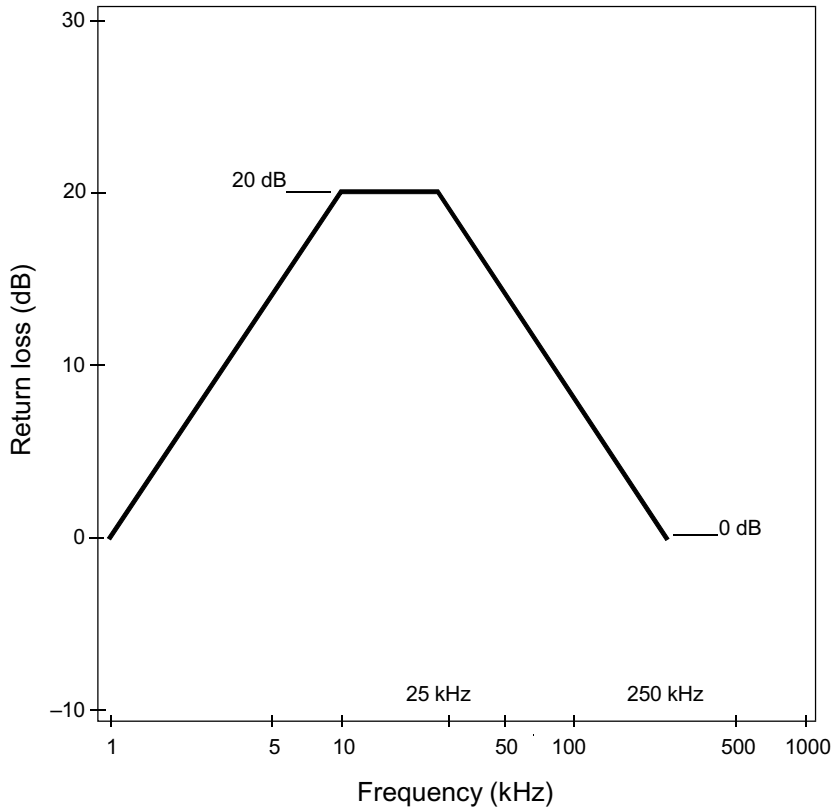

Figure 3: *Minimum return loss*

3.3 Longitudinal conversion loss

The minimum longitudinal balance is as shown in the following figure (in accordance with ITU-T G.961, Appendix II §II.13.3.).

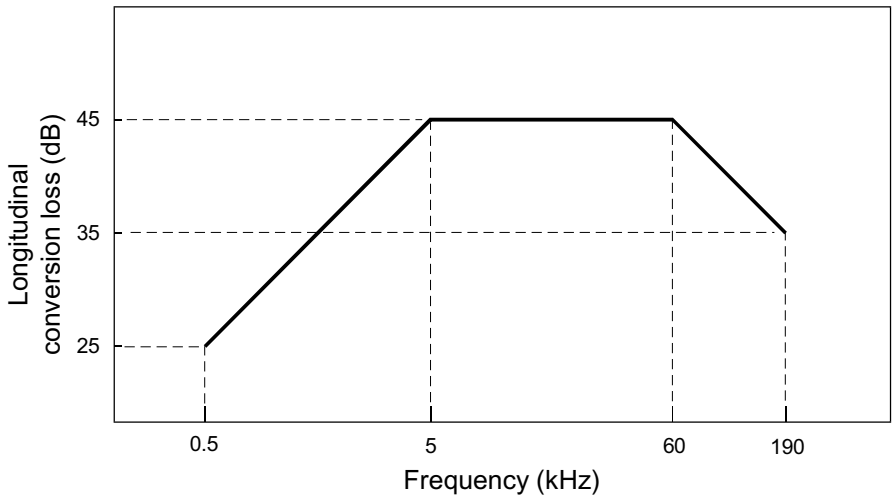

Figure 4: *Minimum longitudinal balance*

4 Jitter

The maximum jitter amplitude at the output network terminal, for single jitter frequencies in the range of 0.1 Hz to 20 kHz, with the bit rate in the range of 80kbaud/s ± 5ppm is as shown in the following figure (in accordance with ITU-T G.961, Appendix II §II.11.).
The maximum wander per day on the NT output is equal to 1.44 UI pp where the maximum rate of phase change is 0.06 UI/hour.

The maximum jitter on the network input port with the bit rate in the range of 80kbaud/s ±5ppm is defined as following:
a) the jitter should be equal to or less than 0.04 UIpp and less than 0.01UIr.m.s. when measured with high-pass filter having a 6 dB/octave roll-off below 80 Hz.
b) the jitter relative to the phase of network input signal should not exceed 0.05 UIpp and 0.015r.m.s. when measured with high-pass filter having a 6 dB per octave roll-off above 40 Hz and below 1.0 Hz.
c) the maximum departure of the phase of the input signal from its nominal difference (long-term average) from the phase of the NT output signal should not exceed 0.1UI.

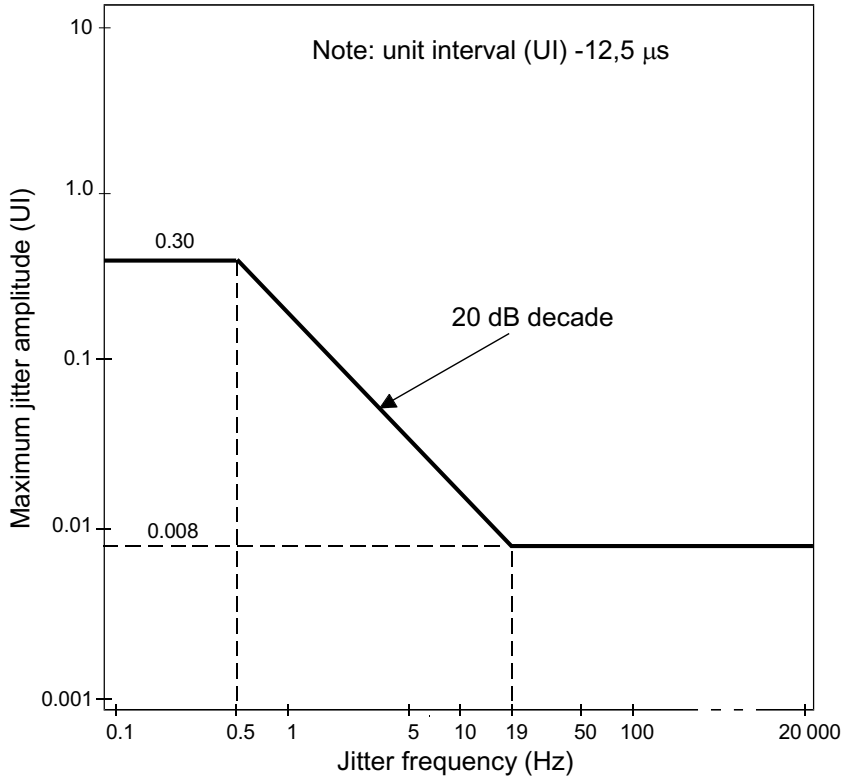

Figure 5: *Maximum jitter tolerances on the NT output*

5 Power supply

Power supply for NT1 and/or regenerator is optional. Voltage source supplying NT1 is a constant voltage source with current limit. Maximum value of the LT output voltage amounts to 120V. Current limit amounts to 50mA (in accordance with ITU-T G.961, §8.6.). The following table presents permissible voltage values on the LT output (in accordance with ETSI ETR 080 §10.5.1).

Minimum [V]	Maximum [V]
51	69
66	70
91	99
90	110
105	115

Table 3: *Voltage ranges for NT1 supply*

5.1 Dynamic power feeding requirements

During application of LT power source test load as shown in the following figure, it is necessary that the circuit generating NT1 supply provides the current of at least X mA for at least 1.5s before activation of current limitation (in accordance with ETSI ETR 080 §10.5.2).

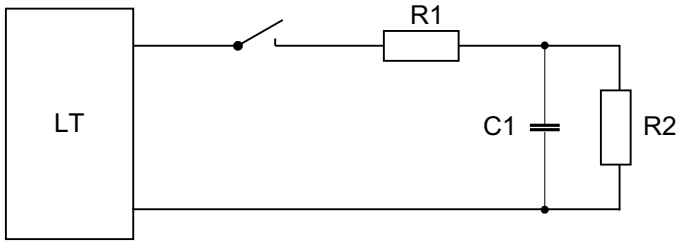

Figure 6: *Power source test load*

The table below presents dependence of X values and component values on LT power source range.

Voltage range	R1[Ω]	C1[μF]	R2[Ω]	X [mA]
51-69	100	200	5000	45
66-70	900	200	1000	40
91-99	1000	400	3000	45
90-110	1000	400	3000	40
105-115	1000	400	3000	40

Table 4: *Component values for power source test load*

5.2 Requests for the reset of NT1 and regenerator

The LT shall provide for reset function a voltage below 5V for at least 2s when measured over a load of 100kΩ connected to the LT terminals.

6 Scrambling

The data stream in each direction of transmission shall be scrambled with a 23rd-order polynomial prior to the insertion of frame word (in accordance with ITU-T G.961, Appendix II §II.9.).
In the LT-NT1 direction the polynomial shall be: $1 \oplus x^{-5} \oplus x^{-23}$

In the NT1-LT direction the polynomial shall be: $1 \oplus x^{-18} \oplus x^{-23}$

$\oplus$ is modulo 2 summation.

7 Frame structure

Each frame contains 2B + D channel, frame word or inverted frame word and CL-channel with M bits for maintenance purposes. The following table demonstrates a 2B+D field structure (in accordance with ITU-T G.961, Appendix II §II.3.).

Data	B1				B2				D
Pairs of bits	$b_{11}b_{12}$	$b_{13}b_{14}$	$b_{15}b_{16}$	$b_{17}b_{18}$	$b_{21}b_{22}$	$b_{23}b_{24}$	$b_{25}b_{26}$	$b_{27}b_{28}$	d_1d_2
Quat	q_1	q_2	q_3	q_4	q_5	q_6	q_7	q_8	q_9
Bits	8				8				2
Quats	4				4				1

Table 5: *2B+D field structure*

A frame contains of 120 quaternary symbols transmitted within a nominally 1.5 ms interval. Frame structure is presented in the table below.

Frame	FW/IFW	12x(2B+D)	C_L
Function	Frame word	2B+D	Overhead
Quats	9	108	3
Quat position	1-9	10-117	118-120
Bits	18	216	6
Bit position	1-18	19-234	235-240

Table 6: *Frame structure*

7.1 Frame length

The number of 2B + D slots in each frame is 12. Each 2B+D field contains 18 bits (in accordance with ITU-T G.961, Appendix II §II.3.1.).

8 Frame word

The frame word is used to allocate bit positions to the B, D, and CL-channels. It may be also used for baud synchronization. (in accordance with ITU-T G.961, Appendix II §II.4.).

8.1 Frame word in LT-NT1 direction

The frame word in LT-NT1 direction in all frames except the first in a multiframe shall be:
FW = +3+3-3-3-3+3-3+3+3
The frame word of the first frame of a multiframe in LT-NT1 direction shall be:
IFW = -3-3+3+3+3-3+3-3-3

8.2 Frame word in NT1-LT direction

The same as in §7.1.

8.3 Frame alignment procedure

A unique frame alignment procedure is not specified.

9 Multiframe

To enable the allocation of the C_L channel bits over more than one frame, a multiframe is used. The start of the multiframe is determined by the inverted frame word (IFW). The number of frames in a multiframe is 8 (in accordance with ITU-T G.961, Appendix II §II.6.).
Multiframe duration is 12ms.

10 Frame offset in directions LT-NT1 and NT1-LT

The NT1 shall synchronize transmitted frames with received frames (LT-NT1 direction). Transmitted frames shall be offset with respect to received frames by 60±2 quaternary symbols (in accordance with ITU-T G.961, Appendix II §II.7.).

11 C_L channel

C_L channel consists of the last three quaternary symbols (6 bits) in each frame of the multiframe (in accordance with ITU-T G.961, Appendix II §II.8.).

11.1 Bit rate

The bit rate of C_L channel amounts to 4kbit/s (in accordance with ITU-T G.961, Appendix II §II.8.1.).

11.2 Structure

48 bits of a multiframe make a C_L channel and are referred to as M bits (in accordance with ITU-T G.961, Appendix II §II.8.2.).
24 bits per multiframe (2 kbit/s) are allocated to an embedded operations channel (EOC).
12 bits per multiframe (1 kbit/s) are allocated to a cyclic redundancy check (CRC) function.
12 bits per multiframe (1 kbit/s) are allocated to other functions and spare bits.

Multiframe structure is presented in the following table:

		Frame	2B+D	C_L bits M_1 - M_6					
	Quat positions	1-9	10-117	118s	118m	119s	119m	120s	120m
	Bit positions	1-18	19-234	235	236	237	238	239	240
Multiframe number	Basic frame number	Frame word		M1	M2	M3	M4	M5	M6

		Frame	2B+D	C_L bits M_1-M_6					
				LT-NT1					
A	1	IFW	2B+D	EOC_{a1}	EOC_{a2}	EOC_{a3}	ACT	1	1
A	2	FW	2B+D	EOC_{dm}	EOC_{i1}	EOC_{i2}	DEA	1	FEBE
A	3	FW	2B+D	EOC_{i3}	EOC_{i4}	EOC_{i5}	1	CRC_1	CRC_2
A	4	FW	2B+D	EOC_{i6}	EOC_{i7}	EOC_{i8}	1	CRC_3	CRC_4
A	5	FW	2B+D	EOC_{a1}	EOC_{a2}	EOC_{a3}	1	CRC_5	CRC_6
A	6	FW	2B+D	EOC_{dm}	EOC_{i1}	EOC_{i2}	1	CRC_7	CRC_8
A	7	FW	2B+D	EOC_{i3}	EOC_{i4}	EOC_{i5}	UOA	CRC_9	CRC_{10}
A	8	FW	2B+D	EOC_{i6}	EOC_{i7}	EOC_{i8}	AIB	CRC_{11}	CRC_{12}
B,C	...								
				NT1-LT					
1	1	IFW	2B+D	EOC_{a1}	EOC_{a2}	EOC_{a3}	ACT	1	1
1	2	FW	2B+D	EOC_{dm}	EOC_{i1}	EOC_{i2}	PS1	1	FEBE
1	3	FW	2B+D	EOC_{i3}	EOC_{i4}	EOC_{i5}	PS2	CRC_1	CRC_2
1	4	FW	2B+D	EOC_{i6}	EOC_{i7}	EOC_{i8}	NTM	CRC_3	CRC_4
1	5	FW	2B+D	EOC_{a1}	EOC_{a2}	EOC_{a3}	CSO	CRC_5	CRC_6
1	6	FW	2B+D	EOC_{dm}	EOC_{i1}	EOC_{i2}	1	CRC_7	CRC_8
1	7	FW	2B+D	EOC_{i3}	EOC_{i4}	EOC_{i5}	SAI	CRC_9	CRC_{10}
1	8	FW	2B+D	EOC_{i6}	EOC_{i7}	EOC_{i8}	1*	CRC_{11}	CRC_{12}
2,3									

Table 7: *Multiframe structure*

Abbreviations used in the previous table mean:

ACT **Act**ivation Bit (set to binary 1 during activation process)
AIB **A**larm **I**ndication **B**it (indicates interruption)
CRC **C**yclic **R**edundancy **C**heck. Calculated over 2B+D channels and M4 C_L channel bits. Bit CRC_1 is MSB bit of cyclic redundancy check.
CSO **C**old **S**tart **O**nly Bit. Used as indication of NT1 transmitter possibility. With cold-start-only provided for NT1, the bit should be set to binary one.
DEA **Dea**ctivation Bit. It is set to binary one to announce deactivation.
EOC **E**mbedded **O**perations **C**hannel.
a Address bits
dm Data/Message indicator
i Data/Message
FEBE **F**ar **E**nd **B**lock **E**rror Bit. Set to binary 0 after reception of errored multiframe.

NTM	**N**T1 in **T**est **M**ode Bit. Zero indicates NT1 test mode.
PS1,2	**P**ower **S**tatus Bit for NT1 feeding. Binary zero indicates power problems.
quat	Quaternary symbol
SAI	**S-A**ctivation **I**ndicator in S/T interface. This bit is optional. It is set to binary one for S/T activity.
UOA	DLL-only-bit. This bit is an optional one. It is set to binary one for S/T interface activation.
1	Bit reserved for future application.
1*	**N**etwork **I**ndication **B**it
2B+D	User data, bits 19-234 in basic frame.
M	C_L channel, bits 235-240 in basic frame.
FW/IFW	Frame word/inverted frame word, bits 1-18 in basic frame.

Multiframe duration is 12ms.
All bits other than the (inverted) frame word are scrambled.

11.3 Protocols and procedures

11.3.1 Error monitoring function

11.3.1.1. CRC

CRC bits are bits M5 and M6 in in frames 3 through 8 of the multiframe (ITU-T G.961, Appendix II §II.8.3.1.1.). The CRC shall be generated in the multiframe and inserted into the bit stream by the transmitter. Receiver calculates CRC over received bits and compares it with the CRC value received in the bit stream. If the two CRCs differ, there has been at least one error in the covered bits in the multiframe.

11.3.2 CRC algorithm

CRC code is computed using the polynomial (ITU-T G.961, Appendix II §II.8.3.1.2.):

$$P(x) = x^{12} \oplus x^{11} \oplus x^3 \oplus x^2 \oplus x \oplus 1$$

where $\oplus$ is modulo 2 summation. CRC code is computed for B, D and M4 bits.

11.3.3 Other C_L channel functions

11.3.3.1. FEBE bit

This bit is mandatory one (ITU-T G.961, Appendix II §II.8.3.2.1.). FEBE shall be set to binary 1 if there are no CRC errors in the multiframe and binary 0 if the multiframe contains a CRC error. The FEBE bit shall be placed in the next available outgoing multiframe, transmitted back to the far end.

11.3.3.2. ACT bit

Mandatory bit (ITU-T G.961, Appendix II §II.8.3.2.3.). ACT bit is M4 bit in the first frame of multiframes transmitted in both transmission directions. ACT bit is used as a part of start-up sequence.

11.3.3.3. DEA bit

Mandatory bit (ITU-T G.961, Appendix II §II.8.3.2.3.). DEA bit is M4 bit in the second frame of multiframes transmitted from the LT to NT1. It is used by LT for NT1 deactivation. To provide reliable detection of the DEA bit during deactivation attempt, it is necessary to transmit the corresponding status (binary ZERO) in at least three successive multiframes before terminating transmission of signal.

11.3.3.4. NT1 power status bits

NT1 power status bits are M4 bits in the second and third basic frames of multiframes transmitted from NT1 to LT (ITU-T G.961, Appendix II §II.8.3.2.4.). These bits are reserved NT power status indication. Their use is optional. When not used, these bits are set to binary one. The following table presents usage of power status bits (ITU-T G.961, Appendix II, Annex A §AII.2.).

	PS1 PS2	Description
Power regular	11	Primary and back-up battery (if provided) power supplies are both regular. Regular power at T reference point (if provided).
Secondary power outage	10	Primary power regular but the battery one (if provided) is unavailable, irregular or marginal. Power at T reference point is regular (if provided).
Primary power outage	01	Primary power is marginal or has failed. Battery power (if provided) is regular. Power at T reference point is below 34V or reversed polarity.
Primary and secondary power outage	00	Primary and battery power (if provided) are marginal or irregular. Power at T reference point (if provided) is less than 34V or reversed polarity. NT1 may cease normal operation in any moment.

Table 8: *NT1 power status bits*

11.3.3.5. NT1 test mode indicator bit

NT1 test mode indicator bit is M4 bit in the fourth basic frame of multiframes (ITU-T G.961, Appendix II §II.8.3.2.5.). Its usage is optional. When not used, this bit is set to binary one. NT1 is considered to be in a test mode (ITU-T G.961, Appendix II, Annex A §AII.3.) when D or any of B channels are involved in a customer locally-initiated maintenance action. While in test mode, NT1 may be unavailable or unable to perform actions requested by EOC channel.

11.3.3.6. CSO bit

CSO bit is M4 bit in the fifth frame of the multiframe (ITU-T G.961, Appendix II §II.8.3.2.6.). The use of this function is optional. When not used, the bit is set to binary zero. It is used to indicate the start-up capabilities of the NT1 transceiver NT1 (ITU-T G.961, Appendix II, Annex A §AII.4.). If NT1 has a cold-start-only transceiver, this bit should be set to binary one.

11.3.3.7. UOA bit

UOA bit is M4 bit in the seventh basic frame of the multiframes transmitted by an LT (ITU-T G.961, Appendix II §II.8.3.2.7.). The use of this function is optional. When not used, this bit is set to binary one. This bit is used to request the NT1 to activate S/T interface (if present) (ITU-T G.961, Appendix II, Annex A §AII.5.). While activating the S/T interface, this bit is set to binary one. Otherwise, this bit should be set to binary zero.

11.3.3.8. SAI bit

SAI bit is M4 bit in the seventh basic frame of the multiframes transmitted by an NT1 (ITU-T G.961, Appendix II §II.8.3.2.8.). It is used to indicate the activity at the S/T interface. Its use is optional. When not used, this bit is set to binary one. If there is an activity (INFO1 or INFO3 at S/T reference point), this bit is set to binary one (in accordance with ITU-T G.961, Appendix II, Annex A §AII.6.). Otherwise it is set to binary zero.

11.3.3.9. AIB bit

AIB bit is M4 bit in the eighth basic frame of the multiframes transmitted by the network toward the NT1 (ITU-T G.961, Appendix II §II.8.3.2.9.). Its use is optional. When not used, this bit is set to binary one. When the transmission path for B1, B2 and D channels has been established all the way to the exchange, this bit is set to binary one (ITU-T G.961, Appendix II, Annex A §AII.7.). Failure or interruption of transmission system transporting B1, B2 and D channels shall result in sending binary zero to NT1 on the place of this bit. Such errors may relate to signal loss, frame alignment loss, transmission terminal failure etc.

11.3.3.10. NIB bit

NIB bit is M4 bit in the eighth basic frame of the multiframes transmitted by NT1 (ITU-T G.961, Appendix II §II.8.3.2.10.). Its use is optional. When not used, it is set to binary one.

11.3.3.11. Reserved bits

All other M4, M5 and M6 bits are reserved for future standardization (in accordance with ITU-T G.961, Appendix II §II.8.3.2.11.). They are set to binary one prior to scrambling.

11.3.4 EOC functions

24 bits per multiframe (2kbit/s) are allocated to EOC (embedded operations channel) functions (in accordance with ITU-T G.961, Appendix II §II.8.3.3.).

11.3.4.1. EOC frame

EOC contains 12 bits synchronized to the multiframe (ITU-T G.961, Appendix II §II.8.3.3.1.). The following table presents an EOC frame.

Bits	3	1	8
Function	Address field	Data/message indicator	Information field

Table 9: *EOC frame structure*

The three-bit address field is used to address up to 7 different locations.

Data/message indicator bit is set to binary one to indicate that the information field contains an operations code; it shall be set to ZERO to indicate that the information field contains numerical data. Information field may encode up to 256 messages.

Exactly two EOC frames are contained in one multiframe.

11.3.4.2. Operation mode

The EOC protocol functions in a repetitive command/response mode (in accordance with ITU-T G.961, Appendix II §II.8.3.3.2.). Three identical properly addressed consecutive messages should be received before an action is initiated.

The network should continuously send properly addressed message. In order to cause the action on the addressed device, the network shall continue sending the message until receiving the three identical consecutive EOC frames from the addressed device to confirm the transmitted EOC frame. The message sending by the NT1 and receipt by the network of three identical consecutive properly-addressed "Unable to Comply" messages denote notification to the network that the NT1 does not support the requested function, at which time the network may abandon its attempt.

The addressed device shall initiate action when, and only when, three identical, consecutive, and properly-addressed EOC frames that contain a message recognized by the addressed

element, have been received. The NT1 should respond to all received messages. The response should be an echo of the received EOC frame towards the network with two exceptions described below. Any reply or echo shall be in the next available EOC frame, which allows a processing delay of approximately 0.75 ms.

If the NT1 does not recognize the message (data/message indicator set to binary one) in a properly-addressed EOC frame, rather than echo, on the reception of the third and all subsequent same correctly-addressed EOC frame, NT1 shall return the Unable to Comply message in the next available EOC frame.

If the NT1 receives EOC frames with addresses other than NT1 address (000), or the broadcast address, it shall, in the next available EOC frame, return an EOC frame toward the network containing the Hold State message and its own address (000).

If an NT1, with no implemented EOC data transfer functions, receives a data byte (Data/message indicator set to binary ZERO) in a properly-addressed EOC frame, rather than echo on the third and subsequent receipts of that same correctly-addressed EOC frame, NT1 shall return the Unable to Comply message in the next available EOC frame.

11.3.4.3. Addressing

NT1 should recognize two addresses: own (000) and broadcast address (111) (in accordance with ITU-T G.961, Appendix II §II.8.3.3.3.). While sending Unable To Comply message, NT1 should use 000 address.

11.3.4.4. Definition of required EOC functions

(in accordance with ITU-T G.961, Appendix II §II.8.3.3.4.)

1) 2B+D loop. This message directs the NT1 to loop the 2B + D data toward the network. This loop may be transparent or non-transparent but in either case will provide synchronization maintained to the NT1.

2) B1 or B2 loop. This message directs the NT1 to loop back a B1 or B2 channel toward the network. This loop is transparent. The function is optional.

3) Return to normal operation. This message is to release all outstanding EOC controlled operations and to reset the EOC processor to its initial state.

4) Unable To Comply. This message confirms that the NT1 has received an EOC message, but the EOC message is not supported by NT1.

5) Request corrupt CRC. This message requests the NT1 to start sending EOC frames containing corrupt CRCs toward the network, until canceled with return to normal.

6) Notify of corrupted CRC: This message notifies the NT1 that the network shall start sending the intentionally corrupted CRCs until cancellation is indicated by return to normal.

7) Hold State. This message is sent by the network to maintain the NT1 EOC processor and any currently active EOC function in their present state. This message may also be sent by the NT1 toward the network to indicate that the NT1 has received a message with an improper address.

11.3.4.5. Codes for EOC functions

Codes for EOC functions are shown in the following table (in accordance with ITU-T G.961, Appendix II §II.8.3.3.5.):

		Origin(o) Destination (d)	
Message	Message code	Network	NT1
2B+D loop	0101 0000	o	d
B1 loop	0101 0001	o	d
B2 loop	0101 0010	o	d
Request corrupted CRC	0101 0011	o	d
Notify of corrupted CRC	0101 0100	o	d
Return to normal operation	1111 1111	o	d
Hold state	0000 0000	d/o	o/d
Unable To Comply	1010 1010	d	o

Table 10: *Codes for EOC functions*

64 EOC messages are reserved for non-standard applications in the following 4 blocks with 16 codes each: 0100 xxxx, 0011 xxxx, 0010 xxxx, 0001 xxxx. Furthermore, 64 EOC are reserved for internal network use in 4 blocks with 16 codes each: 0110 xxxx, 0111 xxxx, 1000 xxxx, 1001 xxxx. All other codes not defined in the previous table or not reserved for non-standard applications or internal network use are reserved for future standardization.

12 Start-up and control

In accordance with ITU-T G.961, Appendix II, §II.10.